SENSYLINK Microelectronics

(CA9541)

2-to-1 I²C/SMBus Master Selector with Interrupt Logic & Reset

CA9541 is a 2-to-1 I²C/SMBus master selector for dual master applications. It supports two masters that can access the same downstream slave devices via the I²C/SMBus interface. It is ideally used in Server and Telecom equipment.

2-to-1 I²C/SMBus Master Selector with Interrupt Logic & Reset

Description

The CA9541 is a 2-channel (2-to-1) I²C/SMBus master selector designed for dual master applications to improve system reliability. The two masters (for example, primary and back-up) are located on separate I²C-buses that connect to the same downstream slave devices. I²C-bus commands are sent by either I²C-bus master and are used to select one master at a time. Either master at any time can obtain control of the slave devices if the other master is disabled or removed from the system. The failed master is isolated from the system and does not affect communication between the on-line master and the slave devices on the downstream I²C-bus.

Two versions are offered for different architectures. CA9541A with no channel selected after start-up, and CA9541B with channel 0 selected after start-up.

The interrupt outputs are used to provide an indication of which master has control of the bus. Interrupt input ($\overline{\text{INT\_IN}}$) collects downstream information and propagates it to the 2 upstream I²C-buses if enabled. $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are also used to let the previous bus master know that it is not in control of the bus anymore and to indicate the completion of the bus recovery/initialization sequence. If the masking option is set, those interrupts can be disabled and do not generate an interrupt.

A bus recovery/initialization if enabled sends nine clock pulses, a NACK, and a STOP condition in order to set the downstream I²C-bus devices to an initialized state before actually switching the channel to the selected master. An interrupt is sent to the upstream channel when the recovery/initialization procedure is completed.

The CA9541 does not isolate the capacitive loading on either side of the device, so the designer must take into account all trace and device capacitances on both sides of the device, and pull-up resistors must be used on all channels.

External pull-up resistors pull the bus to the desired voltage level for each channel, like 1.8V, 2.5V or 3.3V, which can communicate with 5.0V parts without any additional protection by connecting external pull-up resistors to desired voltage. All I/O pins are 6.0 V tolerant.

Internal power-on reset or forcing low logic at $\overline{\text{RESET}}$ pin will let the chip to be initialized and reset the I²C-bus state machine, configure the chip to its default state.

Available Package: SOP-16, TSSOP-16, QFN4x4-16 package.

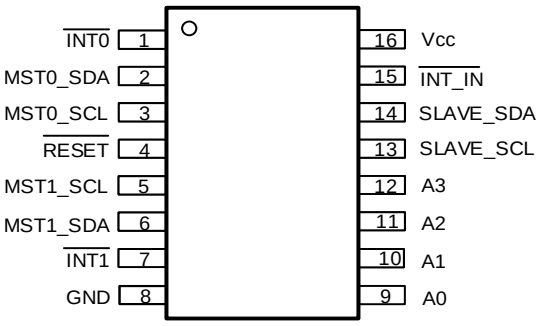
Features

- Operation Voltage: 1.8V to 5.5V
- Standby Current: 13uA @Vcc=3.3V(Typ.)
- 2-to-1 bidirectional master selector
- Compatible with SMBus and I²C interface
- I²C Speed up to 1.1MHz (Fast mode+)
- Interrupt input with active low ($\overline{\text{INT\_IN}}$)
- Interrupt output with active low ($\overline{\text{INT0}}$, $\overline{\text{INT1}}$)
- Reset input with active low ($\overline{\text{RESET}}$)
- 4 address pins allowing up to 16 devices on the I²C-bus
- Channel selection via I²C/SMBus
- Bus initialization/recovery function
- Bus traffic sensor
- Low Ron switches
- Voltage level translation between 1.8V, 2.5V, 3.3V and 5.0V
- Software identification for both masters
- 6.0V tolerant inputs
- Supports hot insertion
- No Glitch during Power-up
- Noise Filter on SCL/SDA inputs
- Temperature Range: -40°C to 85°C
- CA9541A powers up with no channel selected and either master can take control of the bus
- CA9541B powers up with Channel 0 selected

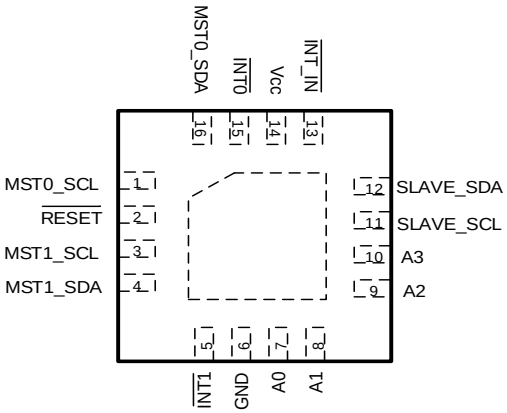
Applications

- Server, Notebook PC
- Telecom equipment
- Dual operating system (low power consumption vs. high performance) smart watch

PIN Configurations (Top View)



SOP-16/TSSOP-16(Package code M/MT)



QFN4x4-16(Package Code QN)

Typical Application

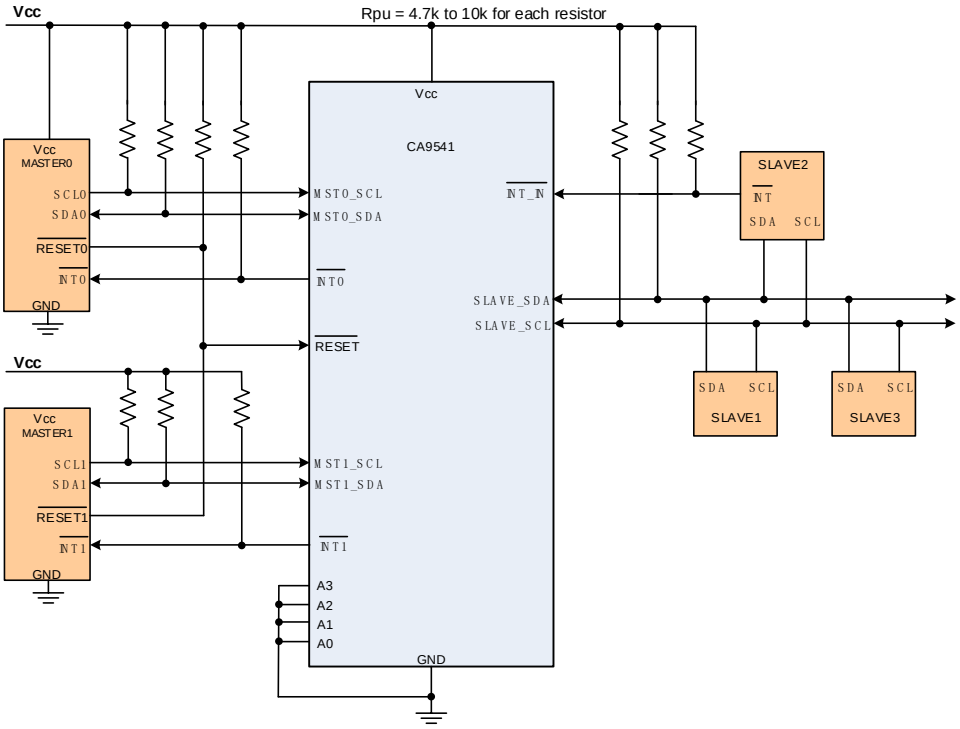


Figure 1 Typical Application of CA9541

Pin Description

PIN Name	PIN No.		Description
	SOP-16 TSSOP-16	QFN4x4-16	
$\overline{\text{INT0}}$	1	15	active LOW interrupt output 0 (external pull-up required)
MST0_SDA	2	16	serial data master 0 (external pull-up required)
MST0_SCL	3	1	serial clock master 0 (external pull-up required)
$\overline{\text{RESET}}$	4	2	active LOW reset input (external pull-up required)
MST1_SCL	5	3	serial clock master 1 (external pull-up required)
MST1_SDA	6	4	serial data master 1 (external pull-up required)
$\overline{\text{INT1}}$	7	5	active LOW interrupt output 1 (external pull-up required)
GND	8	6	ground pin.
A0	9	7	address input 0 (externally held to GND or V_{CC})
A1	10	8	address input 1 (externally held to GND or V_{CC})
A2	11	9	address input 2 (externally held to GND or V_{CC})
A3	12	10	address input 3 (externally held to GND or V_{CC})
SLAVE_SCL	13	11	serial clock slave (external pull-up required)
SLAVE_SDA	14	12	serial data slave (external pull-up required)
$\overline{\text{INT\_IN}}$	15	13	active LOW interrupt input (external pull-up required)
Vcc	16	14	supply voltage

Function Block

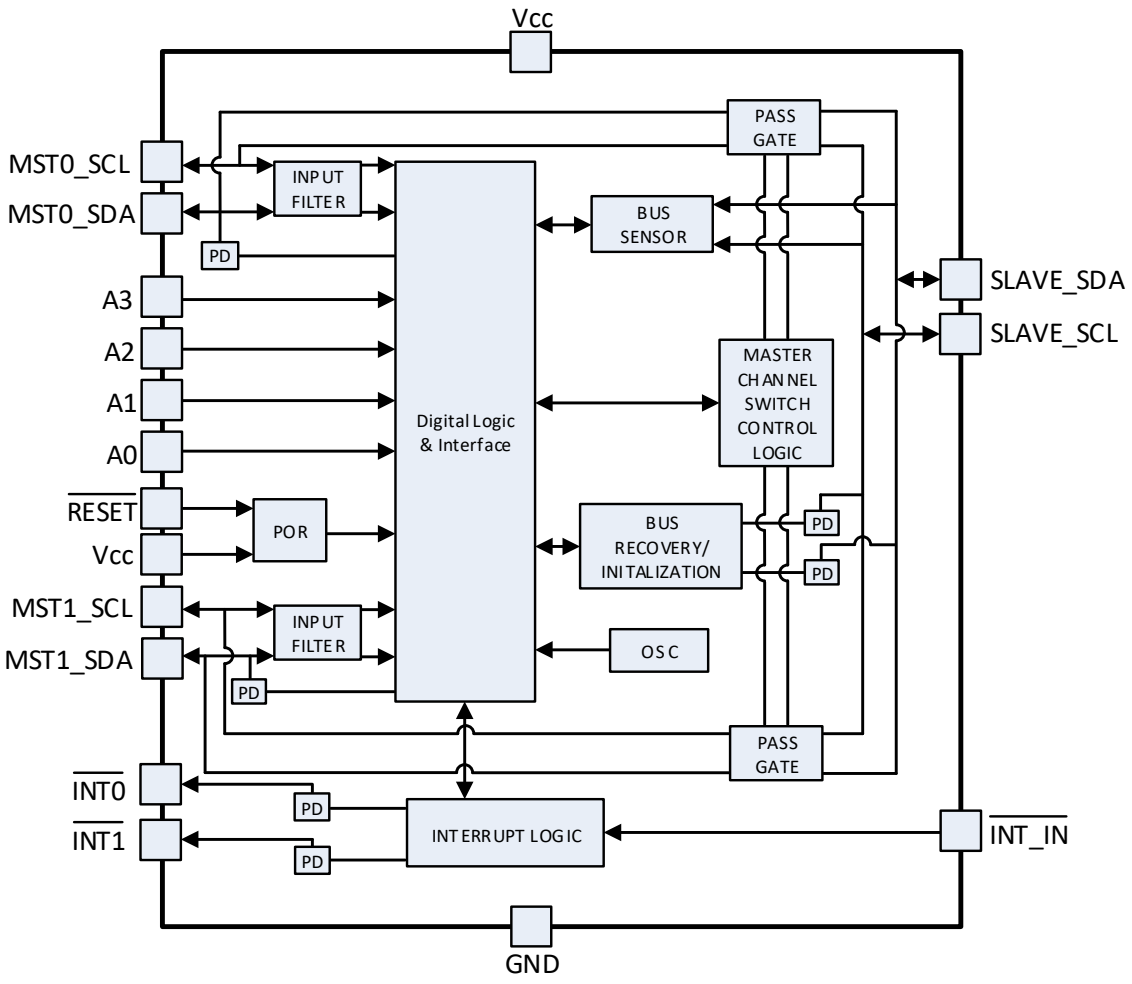
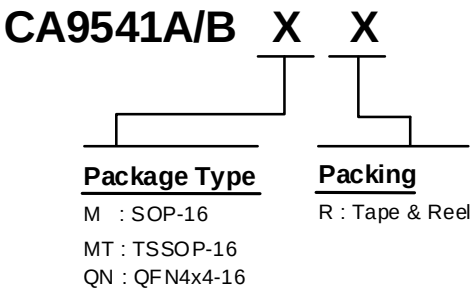


Figure 2 CA9541 function block

Ordering information



Order PN	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
CA9541AMR	Halogen free	SOP-16	9541A YWWAXX	Tape & Reel	4,000	-40°C ~ +85°C
CA9541AMTR	Halogen free	TSSOP-16	9541A YWWAXX	Tape & Reel	4,000	-40°C ~ +85°C
CA9541AQNR	Halogen free	QFN4x4-16	9541A YWWAXX	Tape & Reel	5,000	-40°C ~ +85°C
CA9541BMR	Halogen free	SOP-16	9541B YWWAXX	Tape & Reel	4,000	-40°C ~ +85°C
CA9541BMTR	Halogen free	TSSOP-16	9541B YWWAXX	Tape & Reel	4,000	-40°C ~ +85°C
CA9541BQNR	Halogen free	QFN4x4-16	9541B YWWAXX	Tape & Reel	5,000	-40°C ~ +85°C

1. Based on ROHS Y2012 spec, Halogen free covers lead free. So most package types Sensylink offers only states halogen free, instead of lead free.
2. Marking ID includes 2 rows of characters. In general, the 1st row of characters is part number, and the 2nd row of characters is date code plus production information and trace code.

SENSYLINK Microelectronics Inc.

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