SENSYLINK Microelectronics

(CA9641)

2-channel I²C-SMBus Master Arbiter

CA9641 is a 2-to-1 I²C master demultiplexer with an arbiter function. It is ideally used in Base Station, Server and Telecom Equipment System etc.

1 Description

The CA9641 is a 2-to-1 I²C master demultiplexer with an arbiter function.

The interrupt outputs are used to provide an indication of which master has control of the bus, and which master has lost the downstream bus. One interrupt input ($\overline{INT\_IN}$) collects downstream information and propagates it to the two upstream I²C-buses ($\overline{INT0}$ and $\overline{INT1}$) if enabled. $\overline{INT0}$ and $\overline{INT1}$ are also used to let the master know if the shared mailbox has any new mail or if the outgoing mail has not been read by the other master. Those interrupts can be disabled and will not generate an interrupt if the masking option is set.

The pass gates of the switches are constructed such that the VCC pin can be used to limit the maximum high voltage, which will be passed by the CA9641. This allows the use of different bus voltages on each pair, so that 1.8 V, 2.5 V, or 3.3 V devices can communicate with 3.3 V devices without any additional protection.

Software reset allows a master to send a reset through the I²C-bus to put the CA9641's registers into the power-on reset condition.

An active LOW reset input allows the CA9641 to be initialized. Pulling the $\overline{RESET}$ pin LOW reset the I²C-bus state machine and configures the device to its default state as does the internal Power-On Reset (POR) function.

Available Package: TSSOP-16, QFN3x3-16 package.

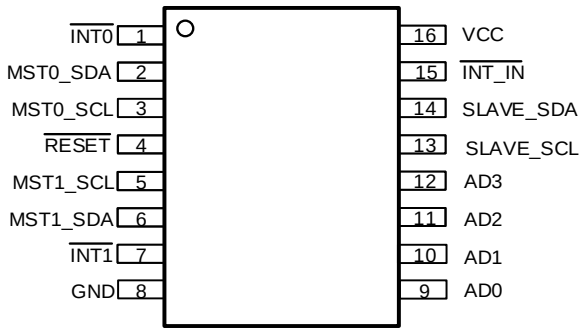
2 Features

- 2-to-1 bidirectional master selector
- Channel selection via I²C-bus
- I²C-bus interface logic; compatible with SMBus standards
- 2 active LOW interrupt outputs to master controllers
- Active LOW reset input
- Software reset
- Four address pins allowing up to 112 different addresses
- Arbitration active when two masters try to take the downstream I²C-bus at the same time
- The winning master controls the downstream bus until it is done, if it is within the reserve time
- Bus time-out after 150 ms on an inactive downstream I²C-bus (optional)
- Readable device ID (manufacturer, device type, and revision)
- Bus initialization/recovery function
- Low Ron switches
- Allows voltage level translation between 1.8 V, 2.3 V, 2.5 V, 3.3 V and 3.6 V buses
- Software identical for both masters
- Operating power supply voltage range of 2.3 V to 3.6 V
- All I/O pins are 3.6 V tolerant
- Up to 1 MHz clock frequency

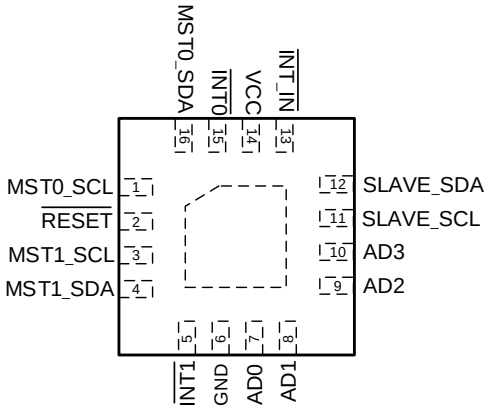
3 Applications

- Server
- Base Station
- Telecom

4 Pin Configurations (Top View)



TSSOP-16(Package Code MT)



QFN3x3-16(Package Code QN)

5 Typical Application

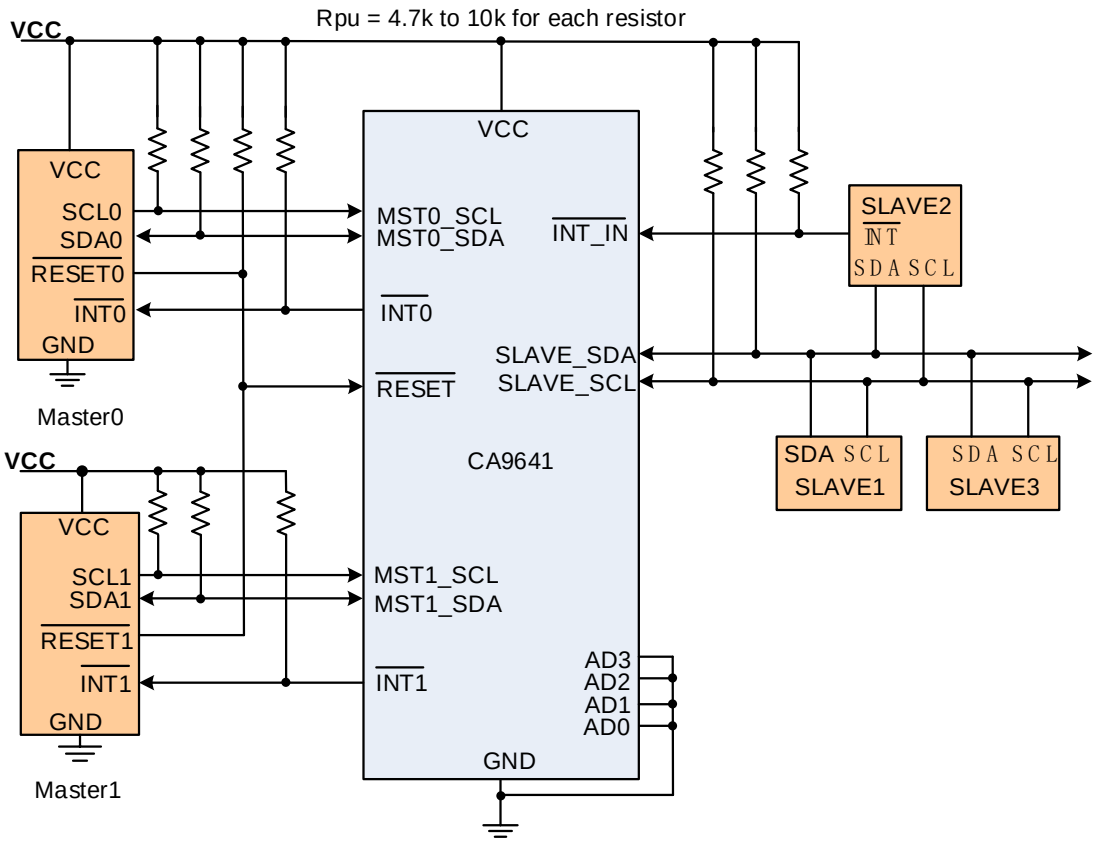


Figure 1 Application of CA9641

6 Pin Description

PIN Name	PIN No.		Description
	TSSOP-16	QFN3x3-16	
$\overline{\text{INT0}}$	1	15	active LOW interrupt output 0 (external pull-up required)
MST0_SDA	2	16	serial data master 0 (external pull-up required)
MST0_SCL	3	1	serial clock master 0 (external pull-up required)
$\overline{\text{RESET}}$	4	2	active LOW reset input (external pull-up required)
MST1_SCL	5	3	serial clock master 1 (external pull-up required)
MST1_SDA	6	4	serial data master 1 (external pull-up required)
$\overline{\text{INT1}}$	7	5	active LOW interrupt output 1 (external pull-up required)
GND	8	6	Ground pin.
AD0	9	7	address input 0 (externally held to GND or VCC, pull-up to VCC or pull-down to GND)
AD1	10	8	address input 1 (externally held to GND or VCC, pull-up to VCC or pull-down to GND)
AD2	11	9	address input 2 (externally held to GND or VCC, pull-up to VCC or pull-down to GND)
AD3	12	10	address input 3 (externally held to GND or VCC, pull-up to VCC or pull-down to GND)
SLAVE_SCL	13	11	serial clock slave (externally held to GND or VCC, pull-up to VCC or pull-down to GND)
SLAVE_SDA	14	12	serial data slave (externally held to GND or VCC, pull-up to VCC or pull-down to GND)
$\overline{\text{INT\_IN}}$	15	13	active LOW interrupt input (external pull-up required)
VCC	16	14	supply voltage

7 Function Block

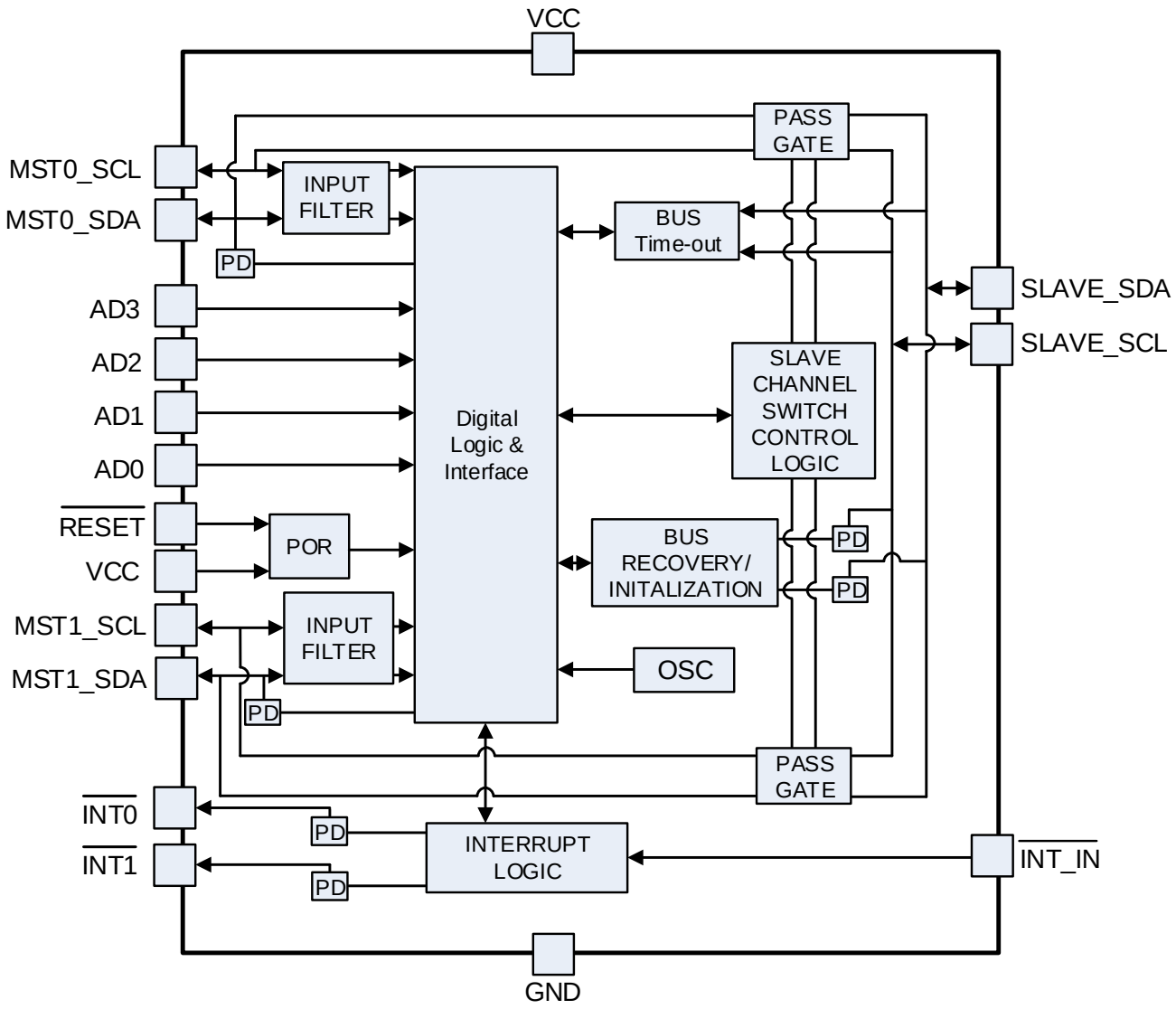
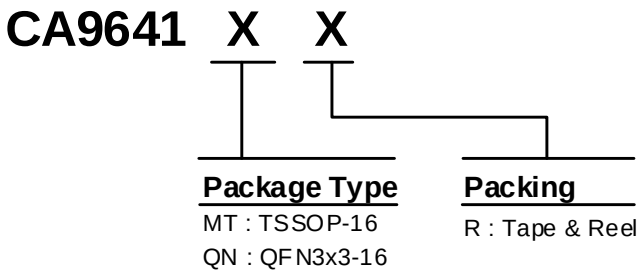


Figure 2 CA9641 Function Block

8 Ordering Information



Order PN	Green[1]	Package	Marking ID[2]	Packing	MPQ	Operation Temperature
CA9641MTR	Halogen free	TSSOP-16	9641 YWWAXX	Tape & Reel	4,000	-40 ºC ~+85 ºC
CA9641QNR	Halogen free	QFN3x3-16	9641 YWWAXX	Tape & Reel	3,000	-40 ºC ~+85 ºC

Notes:
[1]. Sensylink can meet RoHS 2.0/REACH requirement. So most package types Sensylink offers only states halogen free, instead of lead free.
[2]. Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

SENSYLINK Microelectronics Inc.

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