SENSYLINK Microelectronics

(CA6408)

Low-Voltage 8-Bit GPIO Expander

CA6408 is an 8-bit remote GPIO expander. It provides remote GPIO expansion for most MCU families via the I²C or SMBus interface.
It is ideally used in Server, Routers, Telecom equipment and Devices with GPIO-Limited MCU.

Low Voltage 8-bit I²C and SMBus I/O Expander with Interrupt, Reset and Voltage-Level Translation

1. Description

The chip is an 8-bit I/O expander. It provides remote GPIO expansion for most MCU families via the I²C or SMBus interface. The CA6408 has 8-bit Input Port register, Output Port register, Configuration register (setup as input or output), and Polarity Inversion register (active high or active low). After power on, the 8 I/O pins are configured as inputs with an internal weak pull-up to V_{CC}. However, the master can enable the I/O pins as either inputs or outputs individually by setup the configuration register bits. If no external signals are applied to the CA6408 I/O pins, the voltage level is high due to the internal pull-up resistors. The data for each input or output is stored in the corresponding input or output port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register.

There are two supply voltages for CA6408: V_{CCI} and V_{CCP}. V_{CCI} provides the supply voltage for the interface at the master side (for example, a microcontroller) and the V_{CCP} provides the supply for core circuits and Port P. The bidirectional voltage level translation in the CA6408 is provided through V_{CCI}. V_{CCI} should be connected to the V_{DD} of the external SCL/SDA lines. This indicates the V_{DD} level of the I²C-bus to the CA6408. The voltage level on Port P of the CA6408A is determined by the V_{CCP}.

The master can reset the chip probably caused by timeout or other improper operation using the reset feature, which resets all registers in their default state and initializes the I²C/SMBus state machine.

The CA6408 open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

Available Package: TSSOP-16, QFN3x3-16 package.

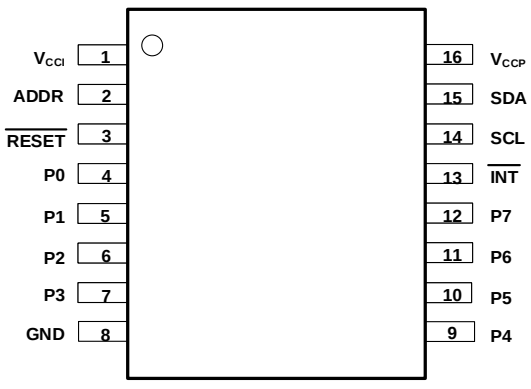
2. Features

- Operation Voltage: 1.65V to 5.5V
- Standby Current: 1.5uA
- 5-V Tolerance I/O Ports
- I²C-bus to parallel port expender
- Compatible with SMBus and I²C interface
- I²C Speed up to 1.0MHz (Fast-mode Plus)
- Up to 2 slave addresses
- Open-drain Interrupt output with active low to indicate input state changed.
- Input, Output, and Configuration Register
- Polarity Inversion Register
- Built-in Power-on Reset
- No Glitch during Power-up
- Noise Filter on SCL/SDA inputs
- Latch feature when driving LEDs directly with high current capability
- Temperature Range: -40℃ to 85℃
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)

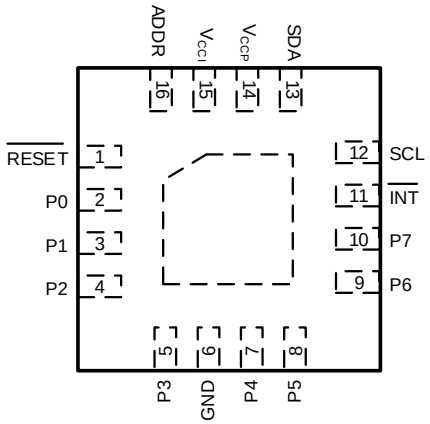
3. Applications

- Server, Notebook PC
- Telecom equipment
- Routers
- Devices with GPIO-Limited MCU
- Automation

4. Pin Configurations

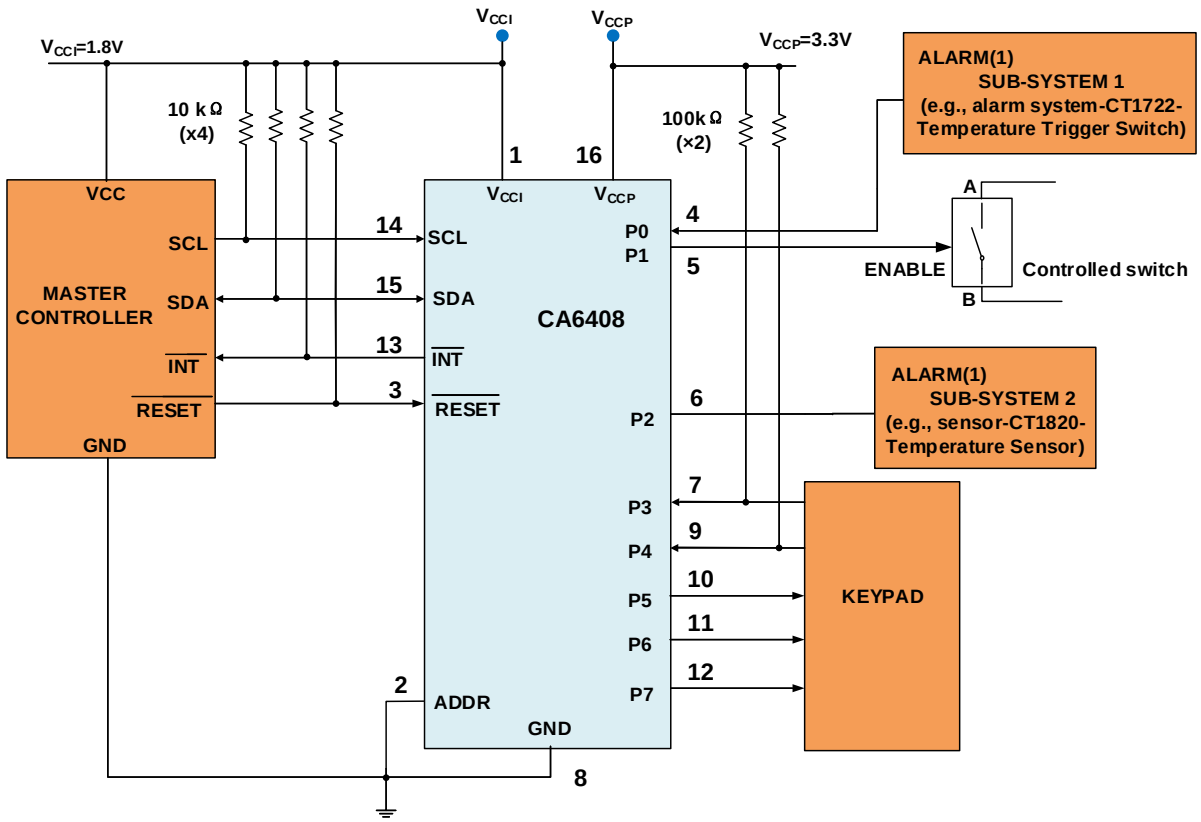


TSSOP-16(Package Code MT)



QFN3x3-16(Package Code QN)

5. Typical Application



Notes:
(1) Device address configured as 010 0000 for this example.
(2) P0 and P2-P4 are configured as inputs.
(3) P1 and P5-P7 are configured as outputs.
(4) External resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed. If an output in the P port is configured as a push-pull output there is no need for external pull-up resistors. If an output in the P port is configured as an open-drain output, external pull-up resistors are required

Figure 1. Typical Application of CA6408

6. Pin Description

Table 1. Pin Description

Pin Name	Pin No.		Description
	TSSOP16	QFN3x3-16	
V_{CCI}	1	15	Supply voltage of I²C-bus. Connect directly to the V_{CC} of the external I²C master. Provides voltage-level translation.
ADDR	2	16	Slave addresses setup pin, which can generate 2 kinds of slave addresses through connect to GND or V_{CCP} respectively.
$\overline{RESET}$	3	1	Active LOW reset input. Connect to V_{CCI} through a pull-up resistor, if no active connection is used.
P0	4	2	P-port input/output (push-pull design structure). At power on, P0 is configured as an input.
P1	5	3	P-port input/output (push-pull design structure). At power on, P1 is configured as an input.
P2	6	4	P-port input/output (push-pull design structure). At power on, P2 is configured as an input.
P3	7	5	P-port input/output (push-pull design structure). At power on, P3 is configured as an input.
GND	8	6	Ground pin.
P4	9	7	P-port input/output (push-pull design structure). At power on, P4 is configured as an input.
P5	10	8	P-port input/output (push-pull design structure). At power on, P5 is configured as an input.
P6	11	9	P-port input/output (push-pull design structure). At power on, P6 is configured as an input.
P7	12	10	P-port input/output (push-pull design structure). At power on, P7 is configured as an input.
$\overline{INT}$	13	11	Interrupt output with active low.
SCL	14	12	Digital interface clock input pin, need a pull-up resistor to V_{CCI}.
SDA	15	13	Digital interface data input or output pin, need a pull-up resistor to V_{CCI}.
V_{CCP}	16	14	Power supply input pin, using 0.1uF low ESR ceramic capacitor to ground.

7. Function Block

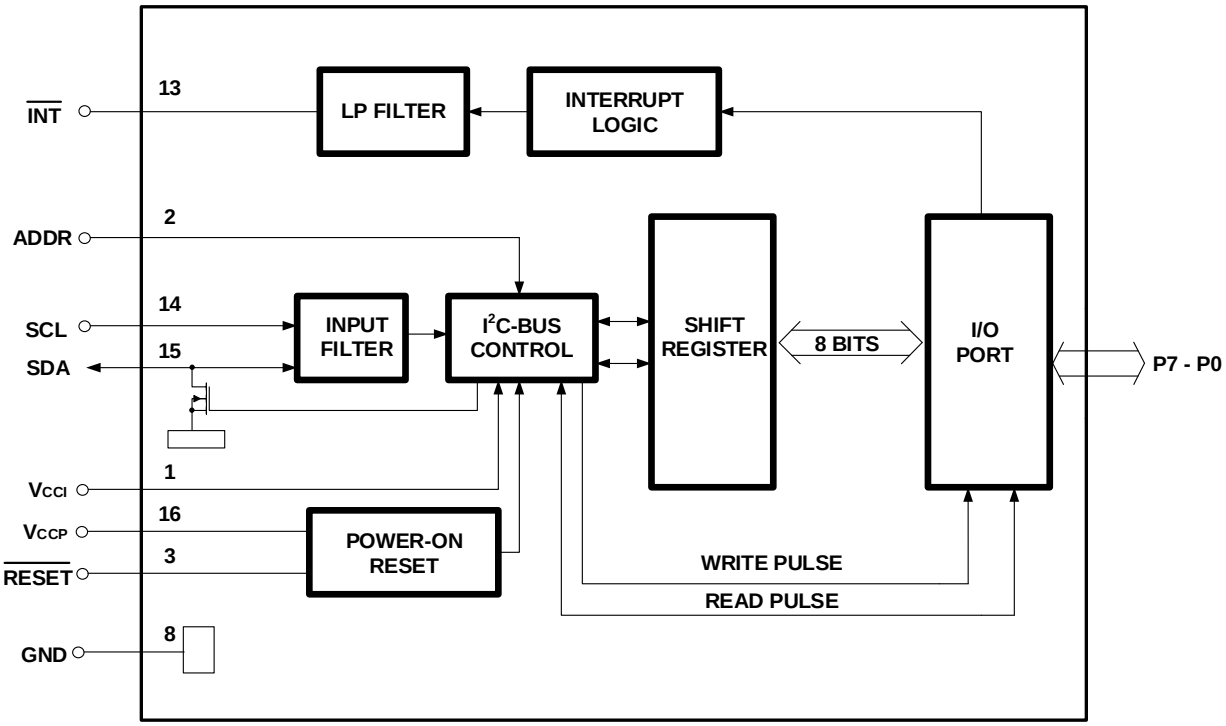
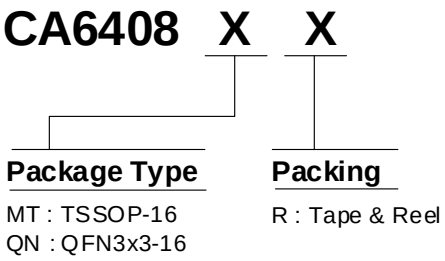


Figure 2. CA6408 Function Block

8. Ordering Information



Order PN	Green(1)	Package	Marking ID(2)	Packing	MPQ	Operation Temperature
CA6408MTR	Halogen free	TSSOP-16	6408 YWWAXX	Tape & Reel	4,000	-40℃ ~ +85℃
CA6408QNR	Halogen free	QFN3x3-16	6408 YWWAXX	Tape & Reel	3,000	-40℃ ~ +85℃

Notes:
(1) Based on ROHS Y2012 spec, Halogen free covers lead free. So most package types Sensylink offers only states halogen free, instead of lead free.
(2) Marking ID includes 2 rows of characters. In general, the 1st row of characters are part number, and the 2nd row of characters are date code plus production information.

SENSYLINK Microelectronics Inc.

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